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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,774	02/12/2002	Menno M. Lindwer	PHN 16,542A	8102

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,774	LINDWER, MENNO M.	
	Examiner	Art Unit	
	William M. Treat	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 15-24 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 15-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. (Patent No. 6,826,749).

4. Patel taught the invention of exemplary claim 15 including a processing device for executing virtual machine instructions; the processing device comprising: an instruction memory for storing instructions including at least one of the virtual machine instructions; a microcontroller comprising a processor comprising a predetermined microcontroller core for executing native instructions from a predetermined set of microcontroller specific instructions; the native instructions being different from the virtual machine instructions; and a pre-processor comprising: a converter for converting at least one virtual machine instruction fetched from the instruction memory into at least one native instruction; and feeding means for feeding native instructions to the microcontroller core for execution; characterized in that the processing device is a stack oriented machine, that at least the top elements of the stack are mapped onto registers of the microcontroller and in that the position of the top of the register stack is indicated using a register of the converter.

1. Claims 15-24 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 15-17 and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. (Patent No. 6,826,749).

4. Patel taught the invention of exemplary claim 15 including a processing device (Fig. 8) for executing virtual machine instructions (JAVA Instructions, Fig. 8); the processing device comprising: an instruction memory for storing instructions including at least one of the virtual machine instructions (inherent or they would be lost while waiting for decoding, etc.); a microcontroller comprising a processor comprising a predetermined microcontroller core for executing native instructions from a predetermined set of microcontroller specific instructions (Fig. 8, microcode from microcode stage (104) being fed to the CPU (101) as native instructions); the native instructions being different from the virtual machine instructions (i.e., Java vs. microcode); and a pre-processor (Fig. 8, Hardware Accelerator) comprising: a converter for converting at least one virtual machine instruction fetched from the instruction memory into at least one native instruction (102 and 104); and feeding means for feeding native instructions to the microcontroller core for execution (106, 112, 120); characterized in that the processing device is a stack oriented machine (114, 113-Stack), that at least the top elements of the stack are

mapped onto registers of the microcontroller and in that the position of the top of the register stack is indicated using a register of the converter (col. 12, lines 12-34).

5. As to claim 16, Patel taught appropriate microcode control of the conversion process (col. 11, lines 43-55).

6. As to claim 17, Patel taught appropriate calculations during the conversion process using top-of-stack value in the converter (col. 12, lines 12-34).

7. As to claims 19 and 20, Patel taught appropriate feeding of the requested instructions after of an interrupt (col. 12, line 61 through col. 13, line 23). The examiner interprets the supplying of the native PC to the Hardware Accelerator by the CPU as a request for refeeding of a number of instructions after the interrupt. Note also that the number of instructions in Patel's reissue buffer is keyed to the depth of the CPU's pipeline which is what applicant discusses as an appropriate number.

8. As to claims 22-23, they fail to teach or define over rejected claims 15, 16, and 17.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (Patent No. 6,826,749).

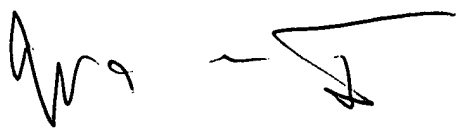
11. Patel teaches the inventions of the independent claims from which claims 18 and 24 depend. And, it is self-evident "bipush-n" is one of the Java codes being converted into native microcode (col. 14, lines 5-15). However, Patel does not specifically teach using MIPS

microcode nor how many microcode instructions he uses. However, the examiner takes Official Notice that if one of ordinary skill in the art can program the conversion using Patel's microcode, then one of ordinary skill can use MIPS microcode to program the same conversion for a MIPS CPU. And, since applicant has taught no new inventive aspect to the MIPS code being used nor some unique programming trick, applicant's code for "bipush n" and that of one of ordinary skill should be equivalent.

12. The examiner regrets that the Patel reference was not published until after his previous action and therefore could not be applied previously.

13. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER